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Design and Fabrication of Large $Al/Al_2O_3/Al$ Josephson Junctions for Metamaterial Arrays

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Abstract

In the emerging field of quantum computing, Josephson Junctions play an important role as components in superconducting qubits. Josephson junctions can also be used to create resonators. Such resonators consists of Josephson junctions coupled in series, as a metamaterial array. These can be used to tune the way qubits interact with the environment, by creating a photonic bandgap. In order to increase the frequency of this bandgap, the junctions in the resonators need to have a lower junction inductance, which can be gained by creating larger Josephson junctions. However, one of the most commonly used fabrications methods, the Manhattan process, cannot be used to reliably produce junctions larger than 600nm x 600nm.

In this report we propose a fabrication technique based on the Manhattan process to allow for fabrication of larger size junctions. Square junctions were designed and fabricated, with side lengths ranging from 1.6 µm to 4 µm. By using a 4-probe technique, the resistance of the fabricated junctions were measured. These measurements indicate that the fabrication of junctions was successful, with sizes ranging up to 4μm x 4μm. For the smallest junctions the measurements showed a higher resistance than expected. This is thought to be the result of a misaligned deposition resulting in smaller junctions than designed.

1 Introduction

Superconducting quantum bits (qubits) are leading candidates in the race to build a quantum computer capable of realizing computations beyond the reach of modern supercomputers[1]. Quantum bits can be created by constructing Josephson tunnel junctions where superconducting electrodes are connected via a thin insulating layer[2]. This creates a barrier which Cooper pairs can tunnel through if the wave-functions of the electrodes overlap[3]. The Josephson junctions in superconducting qubits are made to act as artificial atoms, where they can be manipulated due to their non-linear inductance. Josephson junctions can also be used for tuning the way in which qubits interact with the environment. By creating a metamaterial consisting of an array of Josephson junctions it is possible to modify the way light propagates through them[4]. This is achieved by creating a large impedance resonator consisting of several Josephson junctions in series, shunted by a capacitor. The important parameters for such a metamaterial are the impedance and the frequency of the photonic bandgap,

$$Z_r = \sqrt{L_r/C_r} \tag{1}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{2}$$

where L_r is the total inductance of the resonator and C_r is the shunt capacitance[4]. For further experiments in this field, increasing the value of ω_r is desired. Since the junctions in the metamaterial are coupled in series, the total inductance is the sum of the junction inductance for each junction. The junction inductance L_J depends inversely on the critical current I_c according to equation 3[2].

$$L_J = \frac{\Phi_0}{2\pi I_c} \tag{3}$$

Another important parameter of a Josephson junction is the Josephson Energy, E_J. This can be determined by the normal resistance, R_N, of the junction as

$$E_J = \frac{\Delta \Phi_0}{4e R_N} \tag{4}$$

where Δ is the superconducting gap, Φ_0 is a single flux quanta and e is the electron charge. Larger junctions have a lower normal resistance R_N resulting in an increase of the junction energy[3]. In addition to this, a large E_J corresponds to a high I_c following equation **??**[2].

$$E_J = \frac{\Phi_0 I_c}{2\pi} \tag{5}$$

So, a large junction has a high E_J which in turn corresponds to a low inductance L_J. By increasing the size of the junctions in the resonators a higher value of ω_r can be achieved, which is desired for this application.

A common way of creating tunnel junctions is the Manhattan fabrication technique. This method is illustrated in Figure 1, where a junction is created at the overlap of two evaporated metal layers with an isolating metal oxide layer in-between.

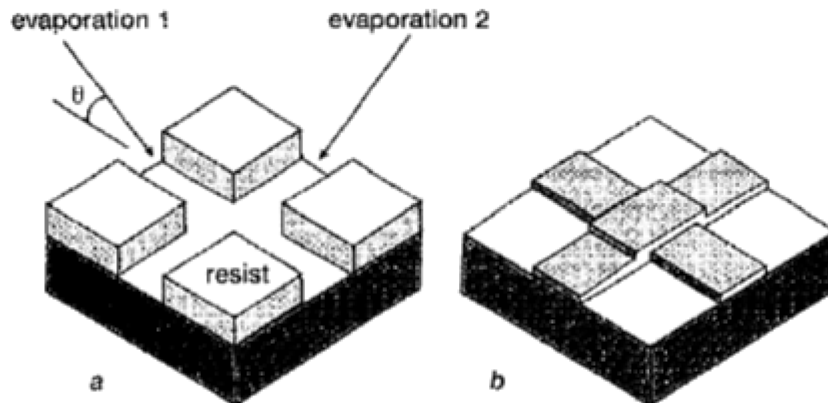


Figure 1: Illustration of the Manhattan process of creating a Josephson junction[5].

The traditional Manhattan process for creating tunnel junctions comes with its limitations. Mainly, the maximum size of the junction is limited by the resist height and angle of deposition[6]. Since a deposition angle of 45°is commonly used, the dimension is regulated by a resist stack height of about 650 nm in order for the metal not to be deposited on the intersecting trenches, see Figure 1a [3].

2 Fabrication

In this report we propose a variation to the Manhattan process that will allow for more reliable fabrication of large junctions. The Manhattan process, which uses a lift-off technique, the width of the resist channels determine the size of the junctions. When fabricating large junctions, metal will also be deposited on the channel walls. During the lift-off, metal on the channel walls will block the resist remover from dissolving the resist. This leads to damaged features. To avoid this a bilayer resist was implemented to create an undercut.

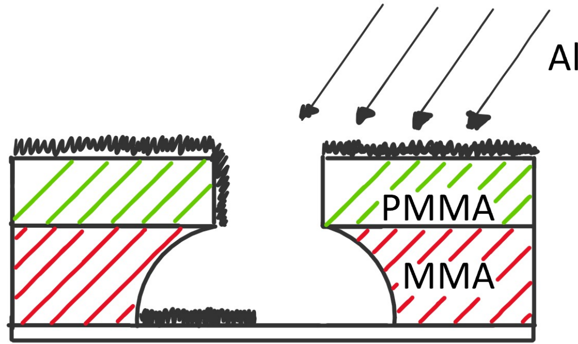


Figure 2: Illustration of the angled deposition of aluminium on a Silicon wafer that has been developed with an undercut layer. The undercut prevents deposition of metal on the whole resist wall.

The bilayer resist consists of a thick MMA layer covered by a thinner layer of PMMA. The designed features was exposed to a high dose e-beam, affecting both the PMMA and MMA layers. Additionally, a low dose e-beam was used to affect only the MMA layer. This creates an undercut as illustrated in Figure 2. During the angled deposition the undercut creates a shading effect that shields parts of the resist layer walls from the deposited metal. Any metal that has been deposited on walls can then be washed away in a lift-off step. The junctions were designed using the software KLayout and a part of the finished design can be seen in figure 3 depicting a junction.

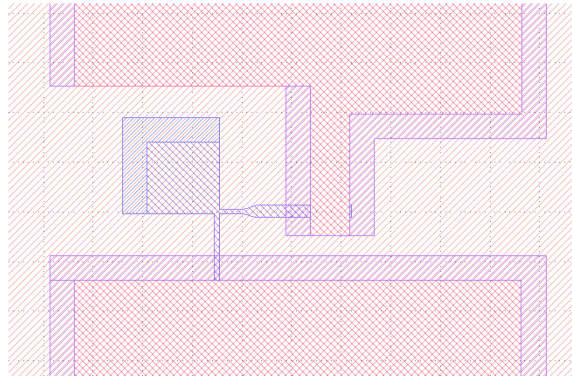


Figure 3: Junction design

The different layers of the junction design were then set to specific exposure parameters, to be able to create an undercut in the lower resist layer around most edges. The larger features of the design, surrounding the Josephson junctions, were made to fit the four-point probe measuring equipment, which was be used to measure the resistance of the junctions.

3 Methods

3.1 Cleaning

A 2 inch wafer was cleaned using the Standard Cleaning process 1. A solution of NH_4OH, H_2O_2 and H_2O in a 1:1:5 ratio was prepared and heated to $80°C$. The wafer was inserted into the solution for 10 min and then rinsed in deionized water using a quick dump rinse (QDR). The wafer was then dipped in HF 2% for 60s and then rinsed in a QDR. To finish the cleaning process, N_2 gas was used to dry the wafer.

3.2 Spin Coating

The wafer was first spin coated with MMA-resist for 60 s at 3000 rpm and acceleration at 1500 ms^{-2}. Using at hotplate at $180°C$ the wafer was baked for 5 minutes. The wafer was then cooled on a coolplate for about 30 s. A second layer consisting of PMMA-resist was then spin coated on top of the MMA for 60 s at 6000 rpm and with an acceleration of 3000 ms^{-2}. The wafer was baked for 5 minutes at $180°C$.

3.3 Electron Beam Lithography

The designed features were patterned onto the wafer using electron beam lithography. For the big features, a dose of $880\mu C/cm^2$ was used. For the Josephson junction, a dose of $800\mu C/cm^2$ was used. In addition a $1\mu m$ region around most features was exposed with a dose of $350\mu C/cm^2$ in order get an undercut.

3.4 Development

The resist pattern was developed in a 1:3 ratio solution of MIBK:IPA for 90 s. The wafer was then moved to pure IPA for an additional 30 s. An optical microscope was used to check the development of the resist.

3.5 Ashing

The wafer was ashed with oxygen-plasma for 15 s at 50 W.

3.6 Deposition

Two layers of Al were deposited from different angles using PVD by evaporation. First, a 50 nm layer of Al was deposited with a rate of 1 nm/s at a 45° tilt. A static oxidation step was performed at 2 mbar and 100 sccm for 20 minutes. The wafer was then rotated 90° around its central axis and a second, 110 nm thick Al layer was deposited with a rate of 1 nm/s at a 45° tilt. Finally, a second static oxidation step was carried out at 10 mbar, 500 sccm for 10 minutes.

3.7 Lift-off

The wafer was placed in a beaker containing Remover 1165 (1-methyl-2-pyrrolidinone) and was heated on a hotplate set to 90° for 10 minutes. After taking the beaker of the hotplate, the sample was left to soak for approximately 72 hours.

The beaker was heated on a hotplate set to 90°. The solution was stirred using a pipette for 25 minutes to remove aluminium and dissolved resist. The sample was moved to a beaker of fresh remover 1165 which was placed in a ultrasonication bath at 35 kHz and 40% power for 5 minutes. The sample was then moved to a beaker of acetone and the ultrasonication step was repeated. After 5 min, the wafer was placed in a beaker of isopropanol and the ultrasonication was once again repeated. Finally, the wafer was blow-dried using N_2.

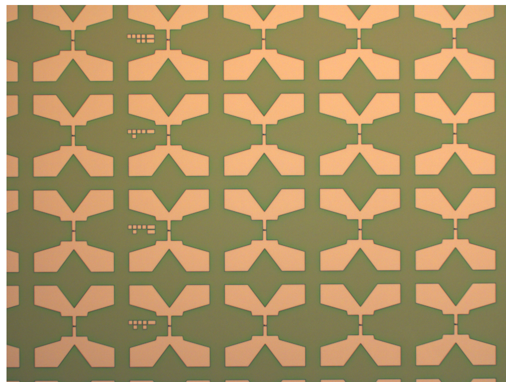
3.8 Measurements

A four-point probe measurement station was used to measure the resistance of the junctions. This probe station uses a four terminal sensing technique and measures the voltage as a function of applied current. Using linear regression, the resistance can be calculated as the slope of the V-I curve according to Ohm's law. The probe station consists of a 2 x 10 array of measuring probes. Meaning ten junctions of the same size could be measured simultaneously. Unfortunately, two of the probes in the array consistently gave unrealistic values for each size. The measurements from two columns in the probe array were therefore excluded, assuming these probes were faulty. In total 8 resistance measurements for each size are included in this report.

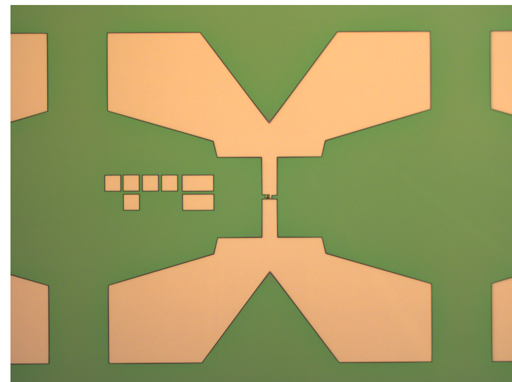
4 Results and discussion

In this section, images taken during the fabrication of junctions using the proposed fabrication technique are be shown. The data gained from the 4-probe measurements will also be presented here, along with correlations relating the junction sizes to their performance.

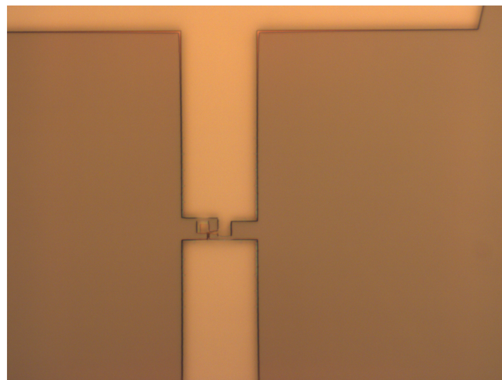
Following the development step, images of the resist were taken using an optical microscope. Figure 4 depicts a junction array as well as a 3.2x3.2µm^2 junction at different magnification.



(a) 5x magnification of junction array.



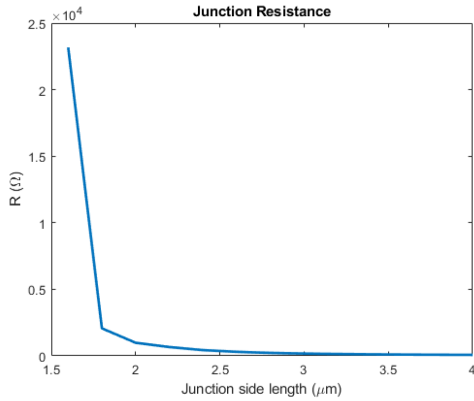
(b) 20x magnification of junction structure.



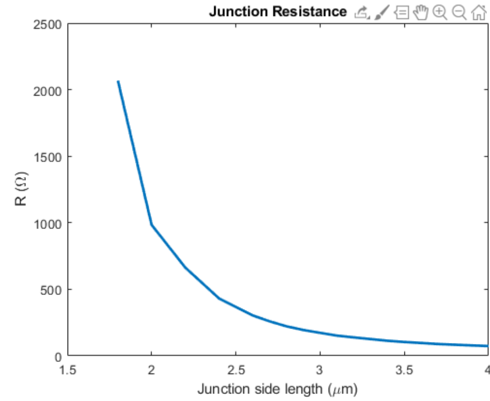
(c) 100x magnification of junction structure.

Figure 4: Microscope images of a 3.2x3.2 µm^2 Josephson junction after development.

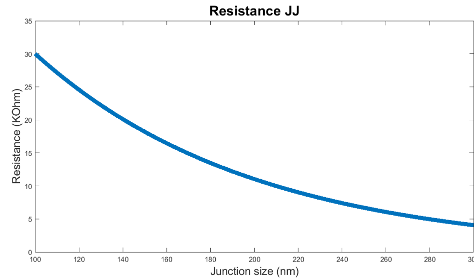
The average measured resistance of the fabricated junction were plotted against the designed junction side length. This graph is shown in Figure 5a. The resistance for the smallest junction is significantly higher compared to the larger ones. In Figure 5b the same resistance to size dependence is plotted excluding the smallest junction. This curve shows an almost exponential size dependence of the resistance. The resistance value for the smallest junction does not follow this exponential dependence. In previous studies the resistance size dependence for smaller junctions has been found to follow an exponential curve as shown in Figure 5c. The average resistance measured for the smallest junction was approximately 25 kΩ. Reading from Figure 5c, this resistance value corresponds to a junction with side length 120nm. The resistance of the junctions designed to have side lengths 1.8 μm and 2 μm also deviates slightly from the exponential dependence seen for the larger junction but this deviation is small compared to that of the 1.6 μm side length junction.



(a) Resistance as a function of the junction side length



(b) Junction resistance as a function of the junction side length.



(c) Resistance as a function of junction side length from previous studies.

Figure 5: Graphs depicting the resistance of the junction's dependence on the side length of the feature. The theoretical value used for reference is presented as well for comparison.

Comparing the design and the microscope images taken of the smallest junction, Figure 6, we can see that the resulting junction differs a bit from the intended design. The square which was supposed to be located at the crossing of the to connectors and make up the junction has been misplaced.

This could be a potential explanation of why the resistance of this junction is much higher than expected. The misplacement of the square might have resulted in the junction consisting only of the overlap between the connectors. This junction would have a side length much smaller than intended which would explain the high resistance.

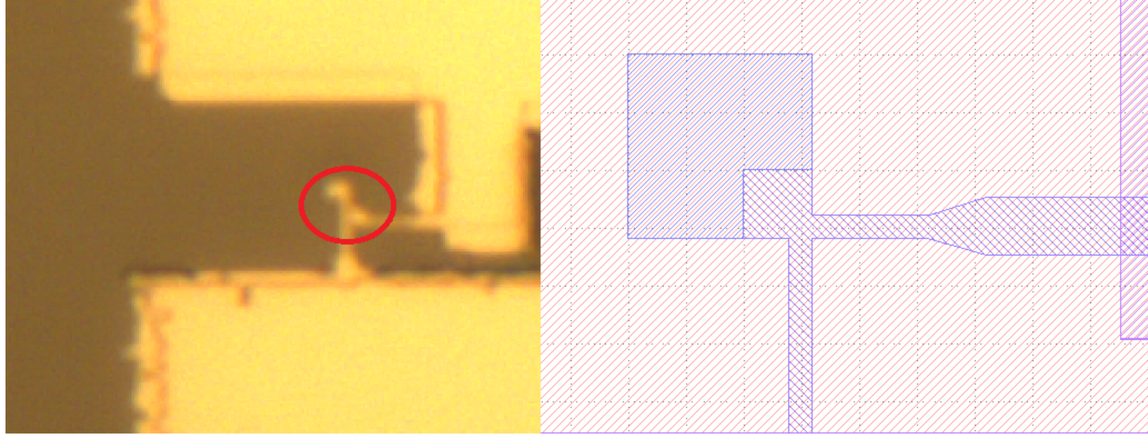
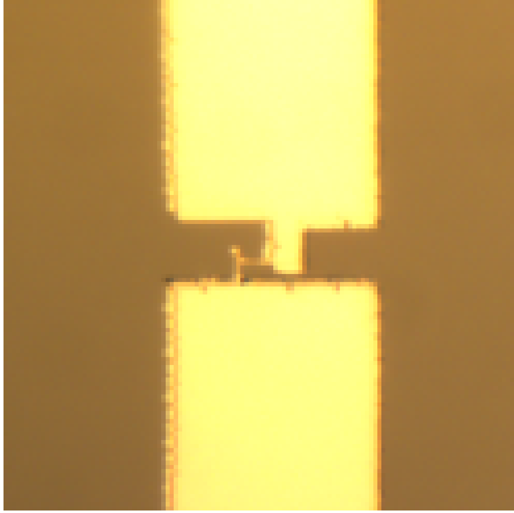
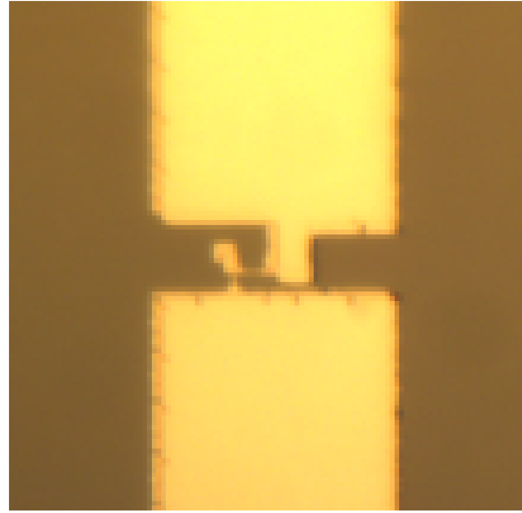


Figure 6: Designed exposure pattern for the smallest junction and the fabricated junction

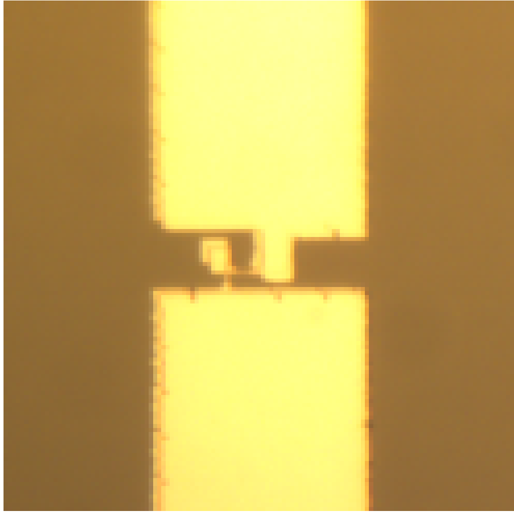
Although the resistance of the larger junctions indicate that the fabrication of the junctions were successful, the microscope images show that they differ slightly from the intended design. Figure 7 show microscope images of different junction sizes. In Figure 7b,c,d we can see that the fabricated junctions have a rectangular shape. However, the rectangular shapes of the fabricated junctions can not be seen in the microscope images taken after development of the exposed resist, Figure 4c. This indicates that the rectangular shape of the deposited metal is due to a fault in the metal deposition step. A possible explanation is that the channels in the resist were not perfectly in parallel with the direction of the evaporation. Due to shadowing effects, such as an angled deposition would lead to a non square junction.



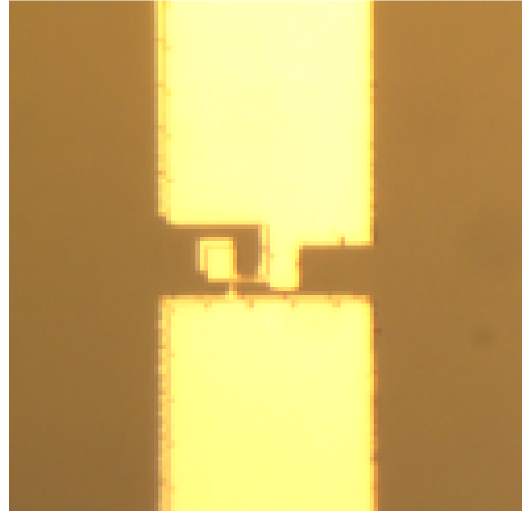
(a) 1.6x1.6µm^2 junction after deposition.



(b) 2.6x2.6µm^2 junction after deposition.



(c) 3.3x3.3µm^2 junction after deposition.



(d) 4x4µm^2 junction after deposition.

Figure 7: 100x magnification of Josephson junctions of varying size, after deposition.

Using the measured resistance, the junction energy can be calculated using equation 4. As seen in Figure 8, a larger junction size resulted in a larger junction energy, E_J, which in turn following equations (5), (3) and (2), would result in a higher photonic bandgap for a superconducting resonator application.

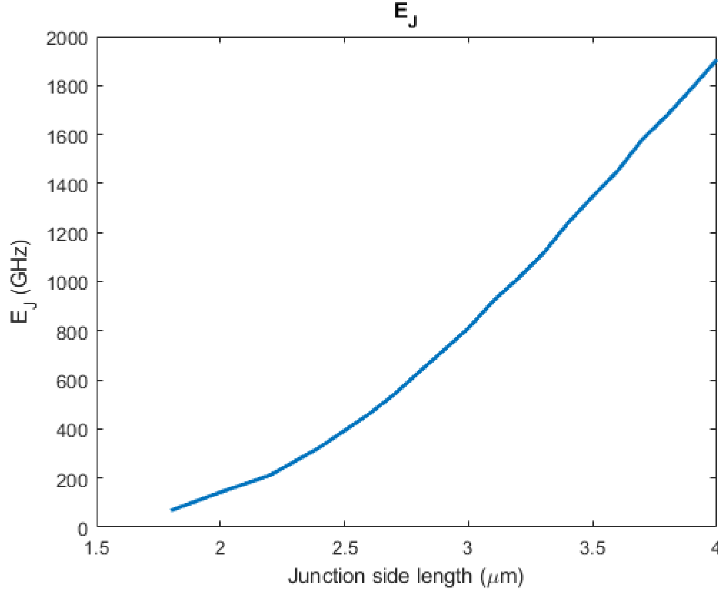


Figure 8: E_J as a function of the junction side length.

5 Conclusions and future outlook

Our proposed method of fabrication was used to fabricate junctions with design sizes ranging from 1.6μm x 1.6μm to 4μm x 4μm. The junctions were successfully deposited and their resistance was within the expected values. However, for the smaller junctions designed to have side lengths from 1.6μm to 2μm the fabricated junction appear to have been malformed, resulting in junctions with significantly smaller sizes than intended. This is likely due to a misalignment of the wafer during the evaporation step. This has also affected the larger size junction resulting in rectangular shaped junctions.

For future studies, more rigorous characterisation of the junctions using scanning electron microscopy or similar methods is suggested to validate the fabrication process. Using these tools, resulting side lengths could more closely be evaluated. Furthermore, exploring the upper and lower bounds of size limitations of this manufacturing process would be of interest. For example, fabrication of junctions with sizes 600-1600nm with the suggested method has not been studied. To do this, the alignment process would need to be optimised to give junctions that better correlate to the intended design. The upper bound would need to be investigated to study the potential maximum photonic bandgap that can be achieved. Additionally, the metamaterials containing these junctions of varying sizes would need to be developed and tested in a low temperature environment.

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